PROPOSED CLAIM AMENDMENT

Please amend the claims in accordance with the following listing.

Listing of Claims:

1. (Currently Amended): A system for communication on a chip, comprising:

an on-chip communication bus including plural tracks; and

a plurality of stations that couple a plurality of on-chip components to the on-chip communication bus;

wherein each station has a dedicated track which it can use to send information to other ~~stations.~~ stations, and a first on-chip component of the plurality of on-chip components and a second on-chip component of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.

2. (Original): A system as in claim 1, wherein the stations use a packet based communication protocol.

3. (Original): A system as in claim 1, wherein the on-chip components include a PCI bridge, a USB component, or an inter-integrated-circuit component.

4. (Original): A system as in claim 1, wherein each station includes:

an initiator that requests permission to transmit outgoing data over a track to another station and that transmits the outgoing data;

an arbiter that evaluates requests from other stations and selects a track on which to receive incoming data; and

a target that receives the incoming data.

5. (Original): A system as in claim 4, wherein the initiator is connected to a grant multiplexor for selecting a grant line.

6. (Currently Amended): A system as in claim 5, wherein the grant multiplexor further comprises plural smaller multiplexors distributed across the chip to facilitate scalability.

7. (Original): A system as in claim 4, wherein the arbiter is connected to a track multiplexor for selecting a track.

8. (Currently Amended): A system as in claim 7, wherein the track multiplexor further comprises plural smaller multiplexors distributed across the chip to facilitate scalability.

9. (Original): A system as in claim 4, wherein each station further comprises a source queue for queuing outgoing data.

10. (Original): A system as in claim 9, wherein the source queue is a first-in-first-out register.

11. (Original): A system as in claim 4, wherein each station further comprises a destination queue for queuing incoming data.

12. (Original): A system as in claim 11, wherein the destination queue is a first-in-first-out register.

13. (Original): A system as in claim 4, wherein each station further comprises:

a source queue for queuing outgoing data, and

a destination queue for queuing incoming data.

14. (Original): A system as in claim 13, wherein the source queue and the destination queue serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components.

15. (Currently Amended): A system as in claim 1, wherein ~~a first and a second on-chip components of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations,~~ the first and the second on-chip components ~~being~~ are selected from a group consisting of a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) interface, an inter-integrated-circuit (I2C) interface, a universal asynchronous receiver transmitter (UART) interface, a data direction register (DDR), a synchronous dynamic access memory (SDRAM), an ethernet interface, and a general input/output (I/O) interface.

16. (Currently Amended): A system as in claim 1, wherein the stations comprise multiplexors that further comprise:

smaller multiplexors distributed across the chip in stages to facilitate scalability;

pipeline storage elements between some of the stages in order to maintain transmission speed when a track must traverse a large number of stages.

17. (Original): A system as in claim 1, wherein each station comprises a watchdog circuit that determines if its station has gone offline.

18. (Previously Presented): A system as in claim 17, wherein if the watchdog circuit determines that its station has gone offline, that watchdog circuit informs a controller connected to the system.

19. (Currently Amended): A method for communication on a chip, comprising the steps of:

communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components; and

communicating between the plurality of stations using an on-chip communication bus including a plurality of tracks;

wherein each station has a dedicated track which it can use to send information to other ~~stations.~~ stations, and a first on-chip component of the plurality of on-chip components and a second on-chip component of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.

20. (Original): A method as in claim 19, wherein the stations use a packet based communication protocol.

21. (Original): A method as in claim 19, wherein the on-chip components include a PCI bridge, a USB component, or an inter-integrated-circuit component.

22. (Original): A method as in claim 19, wherein the step of communicating between the plurality of stations further comprises the steps of:

sending a request from a first station to a second station;

evaluating the request at the second station;

sending a grant signal from the second station to the first station;

selecting a track at the second station;

sending a data or command from the first station to the second station; and

receiving the data or command at the second station.

23. (Original): A method as in claim 22, wherein

sending the request is performed by an initiator at the first station;
evaluating the request is performed by an arbiter at the second station;
sending the grant signal is performed by the arbiter at the second station;
selecting the track is performed by the arbiter at the second station;
sending the data or command is performed by the initiator at the first station; and
receiving the data is performed by a target at the second station.

24. (Original): A method as in claim 23, wherein the initiator is connected to a grant multiplexor for selecting a grant line.

25. (Currently Amended): A method as in claim 24, wherein the grant multiplexor comprises plural smaller multiplexors distributed across the chip to facilitate scalability.

26. (Original): A method as in claim 23, wherein the arbiter is connected to a track multiplexor for selecting a track.

27. (Currently Amended): A method as in claim 26, wherein the track multiplexor comprises plural smaller multiplexors distributed across the chip to facilitate scalability.

28. (Original): A method as in claim 23, wherein each station further comprises a source queue for queuing outgoing data.

29. (Original): A method as in claim 28, wherein the source queue is a first-in-first-out register.

30. (Original): A method as in claim 23, wherein each station further comprises a destination queue for queuing incoming data.

31. (Original): A method as in claim 30, wherein the destination queue is a first-in-first-out register.

32. (Original): A method as in claim 23, wherein each station further comprises:

a source queue for queuing outgoing data, and

a destination queue for queuing incoming data.

33. (Original): A method as in claim 32, wherein the source queue and the destination queue serve to separate a first clock domain for the on-chip communication bus from a second clock domain for one of the plurality of on-chip components.

34. (Currently Amended): A method as in claim 19, wherein ~~more than one of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.~~ the first and the second on-chip components are selected from a group consisting of a peripheral component interconnect (PCI) bridge, a universal serial bus (USB) interface, an inter-integrated-circuit (I2C) interface, a universal asynchronous receiver transmitter (UART) interface, a data direction register (DDR), a synchronous dynamic access memory (SDRAM), an ethernet interface, and a general input/output (I/O) interface.

35. (Currently Amended): A method as in claim 19, wherein the stations comprise multiplexors that further comprise smaller multiplexors distributed across the chip in stages to facilitate scalability, and pipeline storage elements between some of the stages in order to maintain transmission speed when a track must traverse a large number of stages.

36. (Original): A method as in claim 19, further comprising the step of determining if a station has gone offline, the step of determining performed by a watchdog circuit for the station.

37. (Original): A method as in claim 36, further comprising the step of informing a controller if the watchdog circuit determines that its station has gone offline.

38. (Currently Amended): A system for communication on a chip, comprising:

means for communicating between a plurality of on-chip components and a plurality of stations coupled to the plurality of on-chip components; and

means for communicating between the plurality of stations using an on-chip communication bus including a plurality of tracks;

wherein each station has a dedicated track which it can use to send information to other ~~stations.~~ stations, and a first on-chip component of the plurality of on-chip components and a second on-chip component of the plurality of on-chip components are coupled to the on-chip communication bus through one of the stations.

39. (Previously Presented) A system as in claim 1, wherein each station comprises a requester circuit capable of sending a request signal requesting grant of use of one of the dedicated tracks for communication with other stations, wherein the request signal incorporates one of a plurality of priority levels.

40. (Previously Presented) A system as in claim 1, wherein each station includes an arbiter circuit capable of receiving a request signal and granting permission to a station that originated the request signal to send information to the station that granted permission over the dedicated track of the station that originated the request signal.

41. (Previously Presented) A system as in claim 40, wherein the request signal incorporates a request priority level, and the arbiter circuit is capable of granting permission based on the request priority level.

42. (Previously Presented) A system as in claim 40, wherein the arbiter circuit is directly connected to at least a subset of the plurality of stations to receive request signals from the stations of the subset, the subset comprising the station that originated the request signal.